(19) Europäisches Patentamt
European Patent Office
Office européen d s brevets

(11) EP 0 967 636 A3

(12) **EUROPEAN PATENT APPLICATION**

(88) Date of publication A3:
19.07.2000 Bulletin 2000/29

(43) Date of publication A2:
29.12.1999 Bulletin 1999/52

(21) Application number: **99304717.4**

(22) Date of filing: **16.06.1999**

(51) Int Cl.[7]: **H01L 21/762**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **16.06.1998 US 98203**

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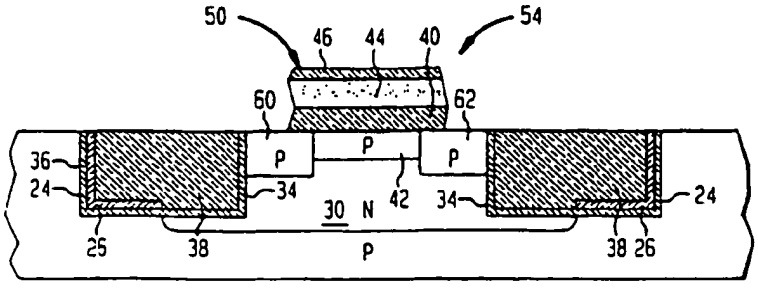
(54) Electrically isolated semiconductor devices

(57) A method for forming a electrically isolated semiconductor devices in a silicon body. A trench is formed in a selected region of the body. A barrier material is deposited over sidewalls of the trench. Portions of the barrier material are removed from a first sidewall portion of the trench to expose such first sidewall portion of the trench while leaving portions of such barrier material on a second sidewall portion of the trench to form a barrier layer thereon. A dielectric material is deposited in the trench, a portion of dielectric material being deposited on the exposed first sidewall portion of the trench and another portion of such deposited dielectric material being deposited on the barrier material. The dielectric material is annealed in an oxidizing environment to densify such deposited dielectric material, the barrier layer inhibiting oxidation of the said second sidewall portion of the trench. A plurality of the semiconductor devices is formed in the silicon body with such devices being electrically isolated by the dielectric material in the trench.

FIG. 3



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EUROPEAN SEARCH REPORT

Application Number
EP 99 30 4717

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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Y	EP 0 441 482 A (ADVANCED MICRO DEVICES INC) 14 August 1991 (1991-08-14) * figure 6 * * column 2, line 49 - column 3, line 18 * * column 4, line 30 - column 6, line 4 *	1-15	
A	US 4 549 927 A (GOTH GEORGE R ET AL) 29 October 1985 (1985-10-29) * column 4, line 1 - line 49 * * column 5, line 67 - column 7, line 2 * * figures 5-9 *	1-15	
A	US 4 894 695 A (ISHII TATSUYA ET AL) 16 January 1990 (1990-01-16) * figures 6D-6G * * figure 7 * * column 3, line 5 - column 4, line 2 * * column 5, line 33 - column 6, line 42 * * column 7, line 63 - column 8, line 9 *	1-3,6,7, 9,10,13	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 May 2000	Giordani, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 30 4717

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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wall portions of the trench.

[0013] For a better understanding of the present invention, and to show how it may be brought into effect, reference will now be made, by way of example, to the accompanying drawings, in which:

FIGS. 1A-1I are diagrammatical cross sectional sketches of electrically isolated MOSFETs at various stages in the fabrication thereof in accordance with the invention;

FIG. 2 is a plan view sketch of one of the MOSFETs shown in FIG. 1I, the cross sectional view of such MOSFET in FIG. 1I being taken along line 1I-1I in FIG. 2; and

FIG. 3 is a cross sectional sketch of the MOSFET shown in FIG. 2, such cross section being taken along line 3-3 in FIG. 2.

[0014] Referring now to FIG. 1A, a semiconductor body or substrate 10, here p-type conductivity silicon, is shown. A layer 12 of silicon dioxide is thermally grown over the upper surface of the substrate 10, here to a thickness in the range of 50A. Next, a layer 14 of silicon nitride is deposited, here by chemical vapor deposition (CVD) to a thickness of here in the range of 2500A on the silicon dioxide layer 14, as shown.

[0015] Referring now to FIG. 1B, a photoresist layer 16 of photoresist is deposited on the layer 14 of silicon nitride and photolithographically patterned, as shown, to have windows 18 formed therein over the regions of the substrate 10 where trenches for the STI are to be formed. Thus, the photoresist layer 16 is patterned to provide an etch mask, as shown in FIG. 1B. The structure is then exposed to an etch, here a dry etch, to first remove the portions of the silicon nitride layer 14 exposed by the windows 18. The photoresist layer 16 is stripped. Next, using the patterned silicon nitride layer 14 as an etch mask, the exposed, underlying portions of the silicon dioxide layer 12 are removed by here a dry etch thereby exposing underlying portions of the surface of the silicon substrate 10. Next, the exposed portions of the silicon are etched, here using a dry etch, to form trenches 20 is the silicon substrate 10 surface as shown in FIG. 1C.

[0016] Referring now to FIG. 1D, a thin layer 24, here 100A thick, of silicon dioxide is thermally grown over the walls 22 (FIG. 1C) of the trenches 20. Next, a barrier material, here a liner, or layer 26 of silicon nitride is deposited over the structure. Here, the silicon nitride layer 26 is deposited by chemical vapor deposition to a thickness in the range of 60A.

[0017] Referring now to FIG. 1E, a photoresist layer 28 is deposited over the surface of the structure and photolithographically patterned, as shown to provide a mask. It is noted that the mask provided by the photoresist layer 28 exposes the regions in the p-type conductivity substrate 10 where n-type conductivity wells 30 are to be formed. It is also noted that the mask provided by the photoresist layer 28 is disposed over sidewall portions 32 of the trenches 20 while such mask has apertures to expose different, sidewall portions 34 of the trench 20. More particularly, the patterned photoresist layer 28 expose the sidewall portions 34 which are disposed about the periphery of the n-type conductivity wells 30, for reasons to become apparent. Suffice it to say here, however, the n-type conductivity wells 30 will have formed therein p-channel MOSFET devices while the regions 36 in the p-type conductive substrate 10 electrically isolated by the trenches 20 will have formed therein n-channel MOSFET devices.

[0018] After patterning the photoresist layer 28 as shown in FIG. 1E, a etch, here a dry etch, is brought into contact with the structure to remove portions of the silicon nitride layer 26 exposed by the apertures in the photoresist layer 28, as shown in FIG. 1E. It is noted that the etch removes the portions of the silicon nitride layer 26 disposed on the trench 20 sidewall portions 34 while the portions of the silicon nitride layer 26 disposed on the trench 20 sidewall portions 32 remain. It is also noted that portions of the silicon nitride layer 26 on the bottom of the trenches 20 exposed by the patterned photoresist layer 28 are also removed while portions of the silicon nitride layer 26 on the bottom of the trenches 20 covered by the patterned photoresist layer 28 also remain.

[0019] Next, a suitable n-type conductivity dopant, here phosphorus, is ion implanted or diffused into the portions of the silicon exposed by the patterned photoresist layer 28 to thereby provide the n-type conductivity wells 30, as shown in FIG. 1E.

[0020] Next, referring also to FIG. 1F, the photoresist layer 28 is stripped away. Next, a silicon dioxide dielectric material 38, here TEOS is deposited over the surface of the structure, portions of such TEOS being deposited in the trenches 20, as shown in FIG. 1F, portion of the material 38, not shown, extending over the silicon nitride layer 14. The structure undergoes a wet anneal during densification of the TEOS material 38. The silicon nitride layer 26 is used to prevent oxygen produced during the wet anneal from entering the portions of the silicon substrate 10 where the n-channel MOSFET devices are to be formed, i.e., the regions 36. That is, the silicon nitride layer 26 prevents oxidation of the silicon trench sidewalls; otherwise, such oxidation would tend to create unwanted stresses and crystal dislocations in the silicon substrate 10. That is, the dielectric material 38 is annealed in an oxidizing environment to densify such deposited dielectric material 38 while the barrier silicon nitride layer 26 inhibits oxidation of the sidewall portions 32 of the trenches 20. It is noted, however, that the sidewall portions 34 disposed about the periphery n-type conductivity wells 30 (i.e, the regions where the p-channel MOSFETs will be formed) do not have the silicon nitride layer 26 thereby eliminating a source of electrons which interfere with the p-channel MOSFETs. The upper portions, not shown, of the TEOS material 38 are removed here by chemical mechanical polishing (CMP)

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to form the structure shown in FIG. 1F.

[0021] Next, the surface of the structure is masked by a photoresist mask, not shown, having windows therein to expose the N-well regions 30 and a p-type conductivity dopant ions, here boron, are implanted through the exposed portions of the silicon nitride layer 14 and silicon dioxide layer 12 to form, after an ion activation anneal, p-type conductivity buried channel regions 42 in the n-type conductivity wells 30, as shown in FIG. 1F.

[0022] Next, the silicon nitride layer 14 and the silicon dioxide layer 12 are removed, here by a wet etch, thereby exposing the surface portions of the silicon substrate 10. Next, referring to FIG. 1G, a layer 40 of silicon dioxide is thermally grown into the exposed surface portions of the silicon substrate 10, as shown. Next, a layer 44 of n+type conductivity doped polycrystalline silicon is deposited over the silicon dioxide layer 44, as shown in FIG. 1H. Next, an electrically conductive layer 46, here aluminum, is deposited over the polycrystalline silicon layer 44, as shown in FIG. 1I. The silicon dioxide layer 40, doped polycrystalline silicon layer 44, and electrically conductive layer 46 are patterned into a gate electrode 50 for the MOSFET devices, as shown in FIGS. 2 and 3 for p-channel MOSFET device 54. Thus, the p-channel MOSFET device 54 has source and drain regions 60, 62. Further, the device 54 is electrically isolated by the dielectric material 38 disposed about the periphery of such device 54. It is also noted that the sidewall portions 34 are not covered with the silicon nitride layer 36. It is noted that, and referring to FIG. 1I, a n-MOSFET device 60 is provided in regions 60 and that such regions are electrically isolated from the regions 30 by trenches having silicon nitride layers 26. Other embodiments are within the spirit and scope of the appended claims.

Claims

1. A method for forming electrically isolated semiconductor devices in a silicon body, comprising:

   forming a trench in a selected region of the body;
   depositing a barrier material over sidewalls of the trench;
   removing portions of the barrier material from a first sidewall portion of the trench to expose such first sidewall portion of the trench while leaving portions of such barrier material on a second sidewall portion of the trench to form a barrier layer thereon;
   depositing a dielectric material in the trench, a portion of dielectric material being deposited on the exposed first sidewall portion of the trench and another portion of such deposited dielectric material being deposited on the barrier material;
   annealing the dielectric material in an oxidizing environment to densify such deposited dielectric material, the barrier layer inhibiting oxidation of the said second sidewall portion of the trench; and
   forming a plurality of the semiconductor devices in the silicon body with such devices being electrically isolated by the dielectric material in the trench.

2. The method recited in claim 1 wherein the forming step comprises forming one of the devices as a buried channel device.

3. The method recited in claim 1 or 2 wherein the step of forming the barrier material comprises forming a barrier material of silicon nitride.

4. The method recited in any preceding claim wherein one of the step of forming the active devices comprises forming the one of the active devices as a p-channel MOSFET and forming another one of the active devices is a n-channel MOSFET.

5. The method recited in any preceding claim wherein the forming step comprises forming one of the p-channel device as a buried channel device adjacent to the first sidewall portion of the trench.

6. The method recited in any preceding claim wherein the forming step comprises the step of depositing a layer of doped polycrystalline silicon over surface portions of the silicon body and patterning such doped polycrystalline silicon body into gate electrodes for the active devices.

7. The method recited in any preceding claim wherein the step of forming the active devices comprises forming one of the active devices as a buried channel device adjacent to the first sidewall portion of the trench.

8. The method recited in any preceding claim wherein the step of forming the buried channel MOSFET comprises forming such MOSFET as the p-MOSFET device.

9. A semiconductor structure, comprising:

   a silicon body;
   a trench disposed in the silicon body, such trench having sidewall portions;
   a barrier material disposed on a second one of the sidewall portions to provide a barrier material lined sidewall portion of the trench, a first one of the sidewalls being un-coated with the barrier material;
   a dielectric material disposed in the trench, one

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portion of the dielectric material being in contact with the barrier material coated second one of the sidewall portions and another portion of the dielectric material being in contact with the first one of the sidewall portions of the trench: a pair of active devices formed in the silicon body, such devices being electrically isolated by the dielectric material in the trench.

10. The structure recited in claim 9 wherein the barrier material is silicon nitride.

11. The structure recited in claim 9 or 10 wherein one of active devices is a p-MOSFET and another one of the active devices is a n-MOSFET.

12. The structure recited in claim 11 wherein one of the devices is a buried channel device.

13. The structure recited in one of claims 9-12 wherein the a layer of doped polycrystalline silicon is disposed over surface portions of the silicon body separated by the dielectric material to provide gate electrodes for the active devices.

14. The structure recited in one of claims 9-13 wherein the one of the active devices the buried channel device is disposed adjacent to the first one of the sidewall portions of the trench.

15. The structure recited in one of claims 1-14 wherein the buried channel device is the p-MOSFET.

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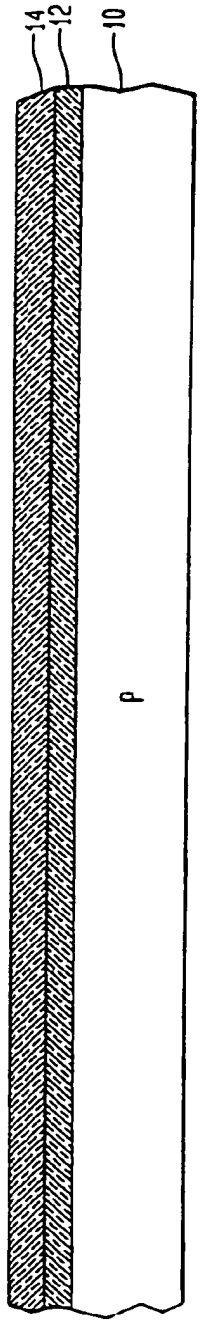

FIG. 1A

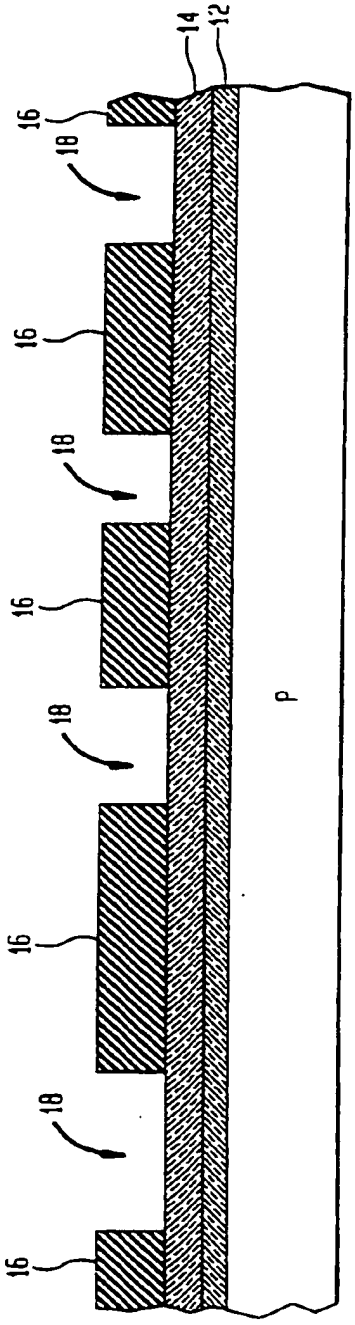

FIG. 1B

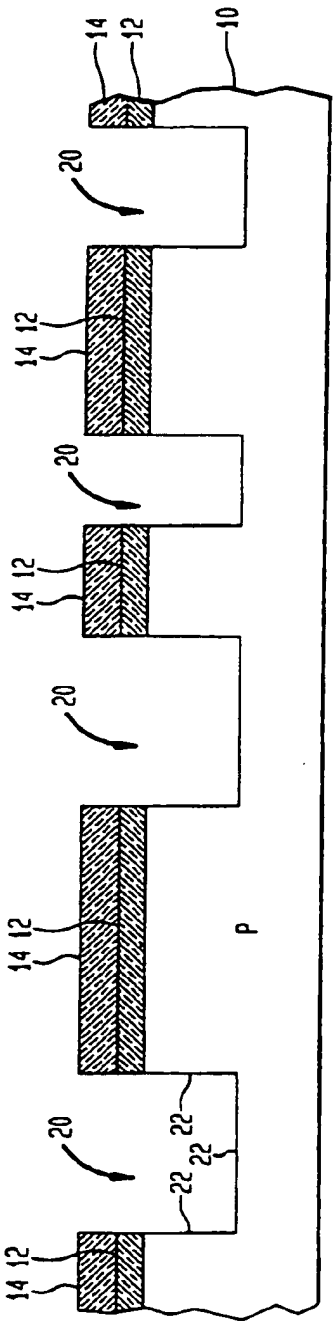

FIG. 1C

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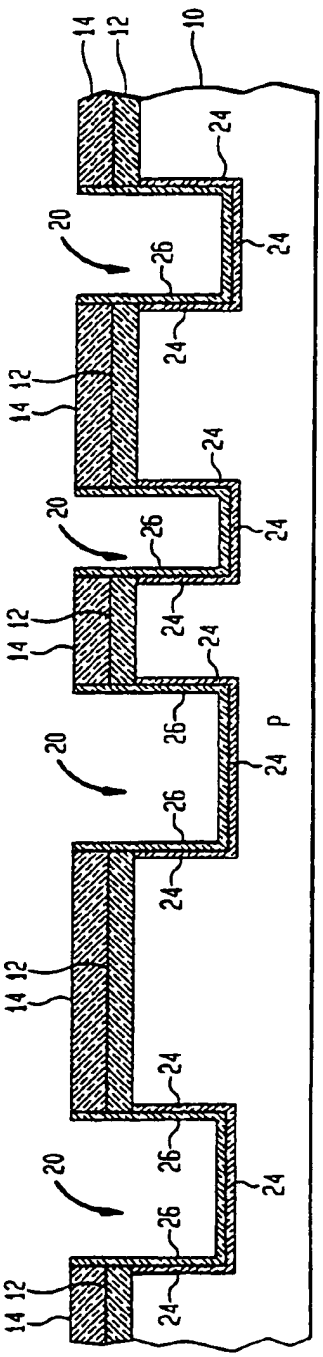

FIG. 1D

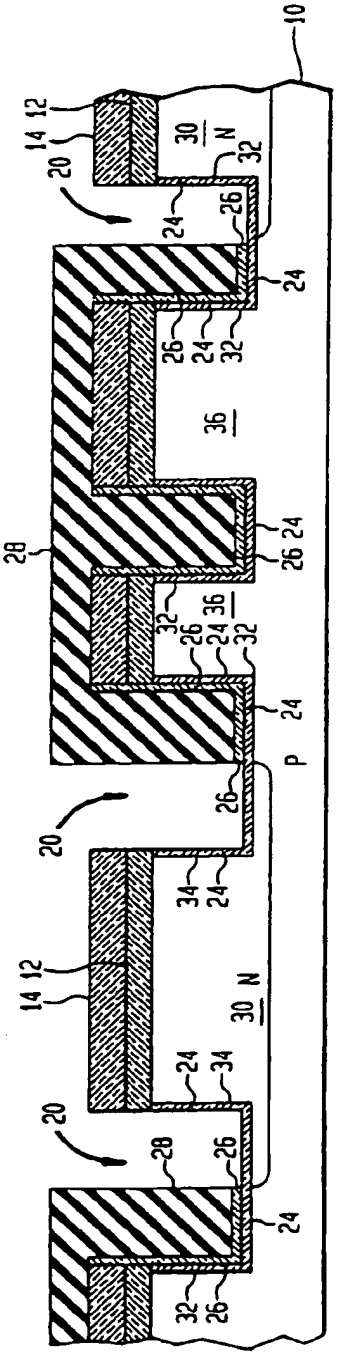

FIG. 1E

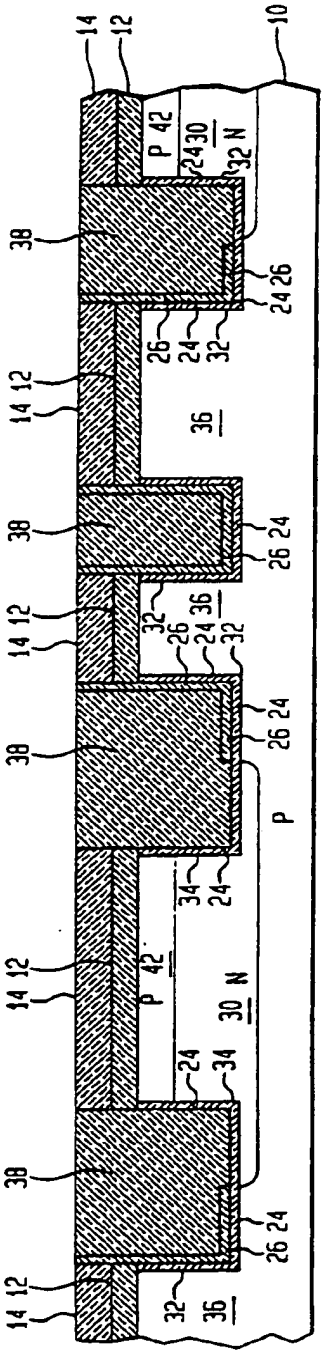

FIG. 1F

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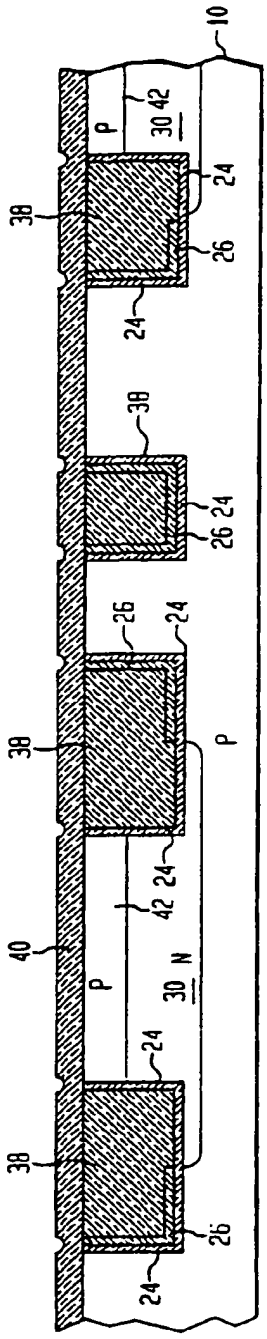

FIG. 1G

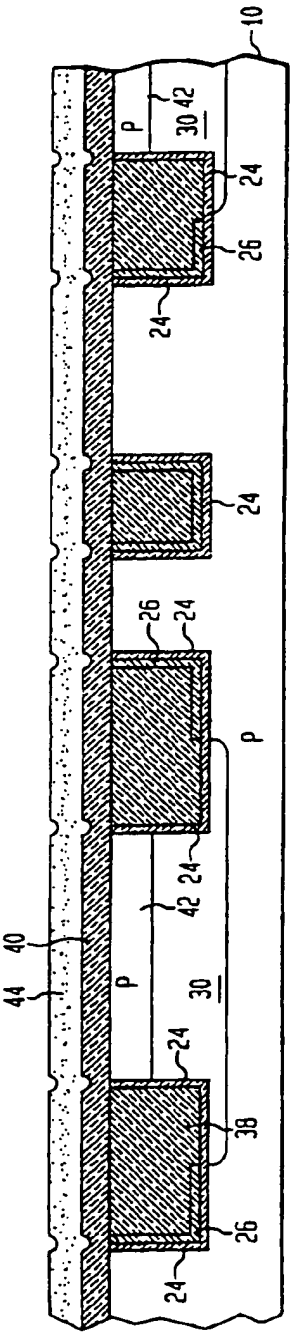

FIG. 1H

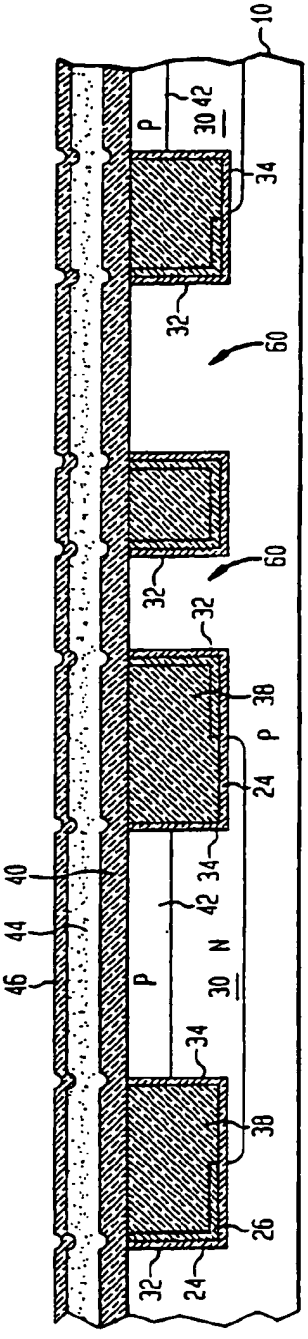

FIG. 1I

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FIG. 2

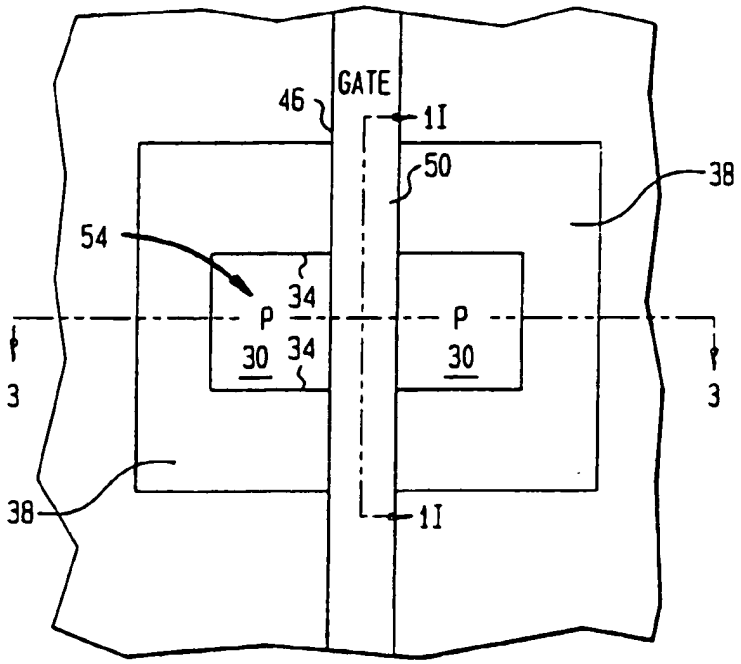
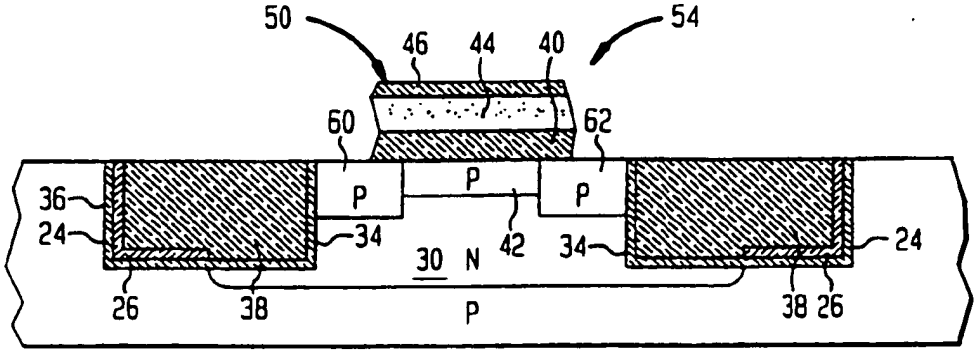


FIG. 3



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